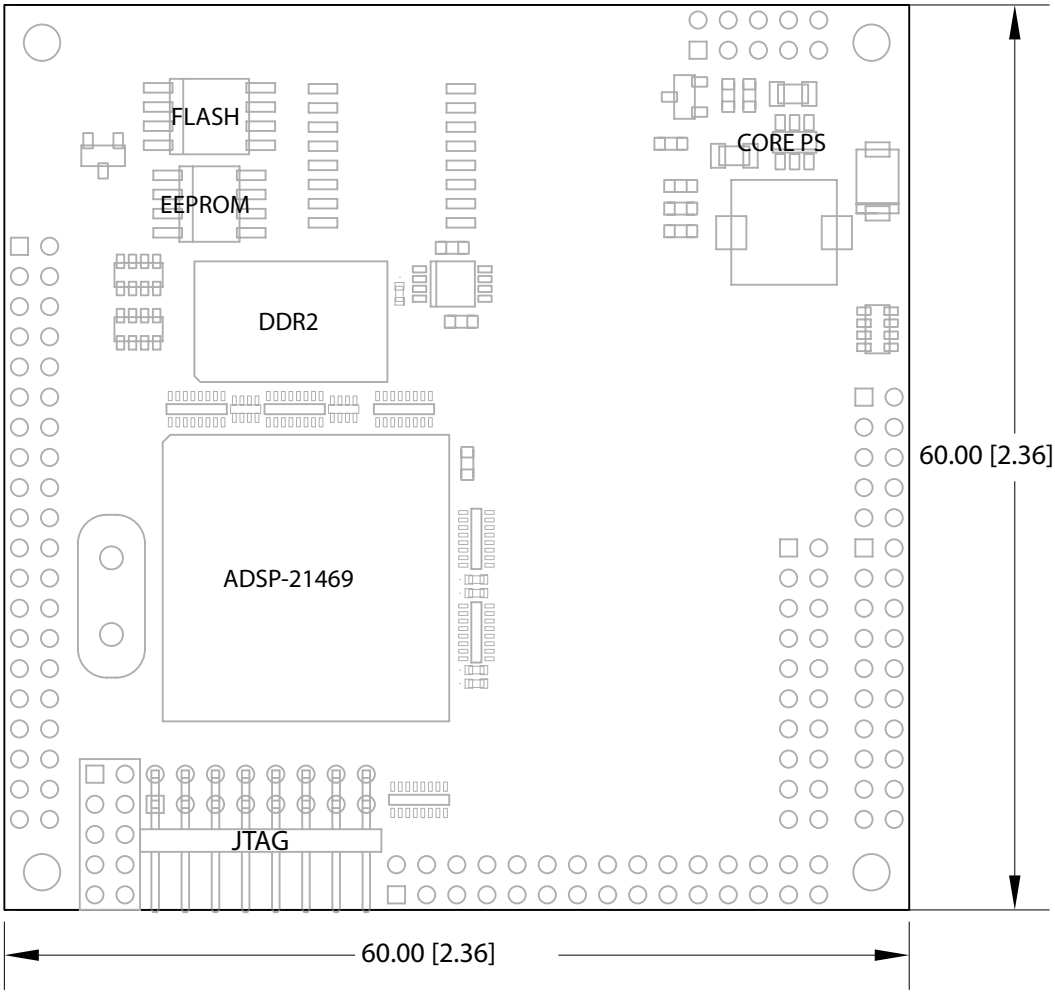
Danville Signal Processing, Inc.

dspblok™ 21469



User Manual

Version 1.01

Danville Signal Processing, Inc.
dspblok™ 21469
User Manual

Copyright © 2009-2010 Danville Signal Processing, Inc. All rights reserved. Printed in the USA.

Under the copyright laws, this manual may not be reproduced in any form without prior written permission from Danville Signal Processing, Inc.

Danville Signal Processing, Inc. strives to deliver the best product to our customers. As part of this goal, we are constantly trying to improve our products. Danville Signal Processing, Inc., therefore, reserves the right to make changes to product specification or documentation without prior notice. Updated operating manuals and product specification sheets are available at our website for downloading.

This manual may contain errors, omissions or "typo's". Please send your comments, suggestions and corrections to:

Danville Signal Processing, Inc.
38570 100th Avenue
Cannon Falls, MN 55009-5534

Trademark Notice

dspblok, dspstak, dspFlash and dspbootloader are trademarks of Danville Signal Processing, Inc.
VisualDSP++, SHARC and Blackfin are trademarks of Analog Devices, Inc.

Contact Information

Danville Signal Processing, Inc.
38570 100th Avenue
Cannon Falls, MN 55009

E-mail: dsp@danvillesignal.com
Web Site: http://www.danvillesignal.com

Voice: 507-263-5854

Fax: 877-230-5629

Table of Contents

Overview 1

dspblok™ Development Boards 1
dspblok™ 21469 1
Intended Audience 2
Getting Started 2

Hardware Overview 5

Power Supply 5
Memory 7
DAI & DPI 7
Data Bus 7
Clocks 7
Link Ports 8
Multiprocessor Configurations 8
Reset 8
Signal Levels 8
Boot Options 8

Connections 9

Connector Recommendations & Notes 11

Connector Specification 11
JH1 – JTAG 11
JH2 – DAI, DPI, IO 11
JH3 – Configuration 11
JH4 – Power & Clock 11
JH5, JH7 – Data Bus 12
JH6 – Link Port 12

Mechanical Dimensions (dspblok 21469) 13

Mechanical Dimensions (dspblok 21469+ICE) 14

Schematic 14

Product Warranty 15

RoHS & WEEE Compliance 16

Overview

Danville Signal's dspblok™ family of products delivers the power of digital signal processing in a small 60mm x 60mm form factor. Connections are brought out to standard 2mm dual row headers. The dspblok reduces development costs, risk and time.

Danville's dspblok DSP function modules are often incorporated directly into larger custom embedded systems. By taking advantage of pretested signal processing modules, pc board layouts become simpler and projects are completed quickly and cost effectively. Danville's dspblok DSP Engines are largely pin compatible. This allows your application to take advantages of new processor technology and extended features in the future.

You can also create small standalone embedded applications by combining a dspblok DSP function module with other dspblok modules. Embedded dspblok systems can be created by using a dspblok power supply such as our dspblok ps-usb, and an I/O module, such as one of our dspblok ad96k family of audio data converter boards. Each board is stacked via 2mm headers to create a low profile configuration where space is at a premium. We also have combination power supply - I/O boards such as our dspblok a9238/48 high-speed ADC boards for SDR applications.

Danville dspblok DSP Engines are the driving force behind many of Danville's standalone products such as our dspstak™, dsprak™, dspMusik™ and dspInstrument™ product lines.

dspblok™ Development Boards

Most dspblok production modules have a companion developer's version, which includes an Analog Devices' EZ-KIT style debugger. These boards are physically larger (60mm x 140mm) to accommodate the debugger but have a matching footprint to our production modules (60mm x 60mm). Once you have developed and debugged your software, you can replace the debugger module (ICE version) with a lower cost, smaller production module.

The dspblok "with ICE" versions include the free Visual DSP++ KIT license and are supported by the FULL version. Depending on the complexity of your application, you may be able to create and support your application without ever needing to purchase additional development tools.

dspblok™ 21469

The dspblok™ 21469 is a highly integrated DSP module that incorporates an Analog Devices' ADSP-21469 SHARC DSP operating at 450 MHz with flash, EEProm and DDR2 SDRAM memory. An onboard switching power supply supports the core voltage requirements of the DSP so that only 3.3V is required to power the dspblok. The ADSP-21469 peripherals include SPORTS (8), SPI(2), TWI (I2C), UART, timers, PWMs, JTAG, an 8 bit wide data bus and LINK ports(2). All of these peripherals are available via 2mm headers on the dspblok.

The dspblok 21469 is also available with USB. See the dspblok 21469+USB manual for specific details.

Intended Audience

The dspblok 21469 requires an understanding of the Analog Devices' ADSP-21469 and the associated tools used for development. If the dspblok 21469 is going to be integrated into a larger hardware design, then it is also assumed that the user is familiar with basic hardware design. In most cases, systems integrators, DSP programmers and software engineers can create DSP embedded systems using our embedded dspblok systems (or dspstak family) without the need for additional hardware design and manufacturing.

If you do not have a background with these skills, you may want to check out our web site (http://www.danvillesignal.com) as well as the Analog Devices web site for links to useful references. Danville engineers are also available to discuss your application.

Getting Started

Danville's customer base is quite diverse. Our customers range from embedded systems hardware designers to system integrators looking for complete turnkey solutions. We often work with embedded systems engineers who may not have specific expertise in digital signal processing.

Regardless of your background, you will need the right tools. We suggest one of the following:

Option 1:

> Start your development with a dspblok 21469+ICE module. The "+ICE" version incorporates an ADI Standalone Debug Agent. You could also use a dspblok 21469+USB+ICE assuming you have clearance for the extra header used for USB. See the dspblok 21469+USB User Manual for mechanical details.
>
> You can use any version of Visual DSP++5.0 for SHARC. There are three basic versions.
>
> The FULL (paid) version supports all SHARC DSPs, Analog Devices standalone emulators, and a simulator. Once you have an Analog Devices FULL license, ADI does not charge for additional maintenance or updates. Of course, this is between you and Analog Devices. Danville is not making any claims on their behalf. You should check the ADI web site for licensing details.
>
> The TESTDRIVE (free) version is exactly the same as a FULL license except that it stops working after 90 days.
>
> The KIT (free) version starts out as a FULL (TESTDRIVE) version but after 90 days requires that the dspblok 21469+ICE is connected via the ADI debug agent. It will not connect to an ADI emulator, simulator or support another SHARC DSP. The linker restricts a user program to 27306 words of memory for code space with no restrictions for data space. The good news is that it can be used to create bootable images (loader files) that can be used with the production dspblok 21469. Depending on your situation, this may be all that you need.

Option 2:

> Start your development with a dspblok 21469 module. In this case, you will want to connect to the dspblok 21469 via an external Analog Devices emulator. Analog Devices offers two versions the USB-ICE and the HPUSB-ICE. We prefer the faster HPUSB-ICE, which is up to 10 times faster and also supports background telemetry. You will also need a Danville JTAG adapter kit (P/N A.08153), which converts the Danville JTAG 2mm header to the larger ADI JTAG connector.
>
> You will also need a FULL VisualDSP++ 5.0 license (at least after 90 days).

You can purchase VisualDSP++ 5.0 and ADI emulators from Danville. We appreciate this business.

If you are designing your own companion board, we strongly recommend that you use one of our existing I/O boards and/or power supply boards as an initial development platform. Depending on your situation, this could be a dspstak system, dspInstrument, or a combination of dspblok I/O and power supply modules. Any of these components will give you a solid footing for development before you incorporate the dspblok into your own target.

If you are laying out your own pc board, we can provide you with PCB footprints and schematic symbols (Gerber & Altium Designer) to help you avoid simple mistakes.

Regardless of your situation, Danville engineers are available to help you with your application. We may have solutions that are not yet on our web site. We also provide many solutions that are specifically tailored to customer needs. Contact us about turnkey solutions.

We recommend that you have the documents:

- Analog Devices ADSP-2146x SHARC Processor Hardware Reference Manual
- Analog Devices SHARC Processor Programming Reference Manual
- Analog Devices VisualDSP++ 5.0 Manual Set

We recommend that you have the tools:

- Analog Devices VisualDSP++ 5.0 for SHARC
- Emulator or Debug Agent (one of the following)
  - Analog Devices HPUSB-ICE and Danville JTAG Adapter P/N A.08153
  - Danville dspblok 21469+ICE or dspblok 21469+USB+ICE

Optional:

- Danville dspFlash Blackfin & SHARC Programmer

Our website (www.danvillesignal.com) has downloads and links to these tools and documents.

The dspblok 21469+ICE includes the following items:

Hardware:

- dspblok 21469+ICE Module
- USB Cable
- Debugger Power Supply (5V, 1A, 5.5/2.5mm coaxial center positive)***

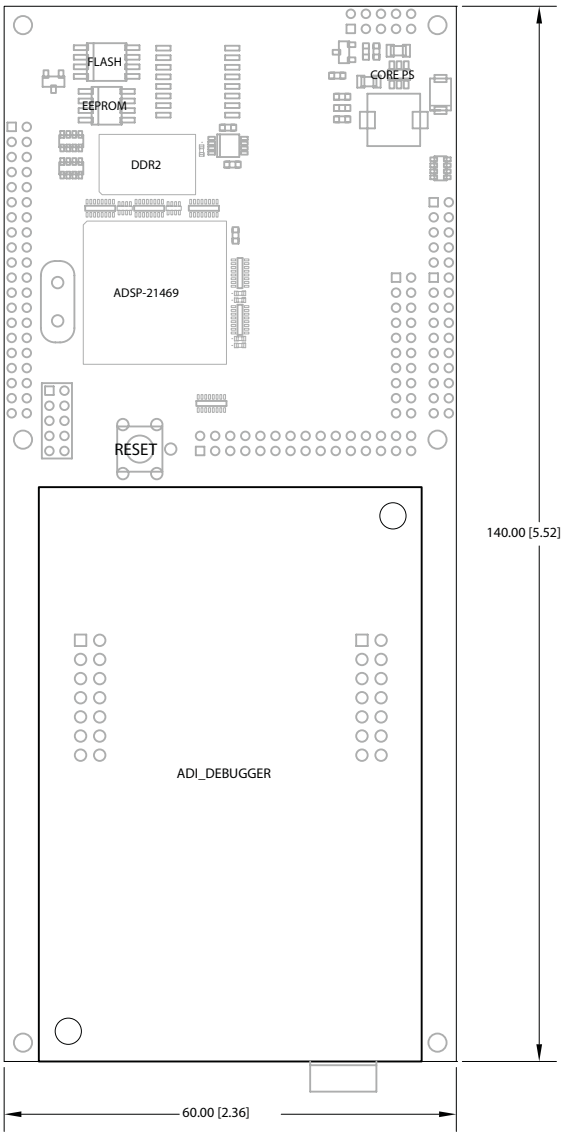
*** North American customers only

Software:

- VisualDSP++ 5.0 for SHARC (KIT license) CD

Documents (CD):

- This Manual
- CAD footprints (Gerber & Altium) formats)
- Schematics
- Sample Programs
- Debug Agent Driver



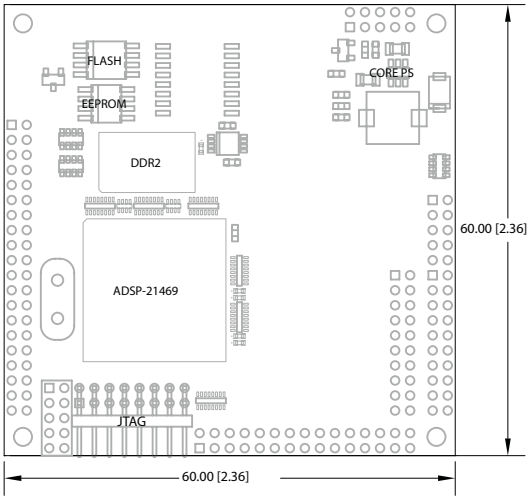
The dspblok 21469 includes the following items:

Hardware:

- dspblok 21469 Module

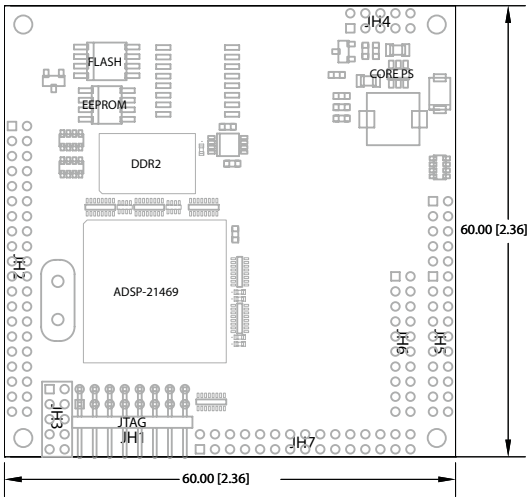
Documents (CD):

- This Manual
- CAD footprints (Gerber & Altium)
- Schematics
- Sample Programs



Hardware Overview

The dspblok 21469 is a small module measuring 60mm x 60mm (2.36″ x 2.36″). JH2 and JH4 - JH7 are 2mm male headers that are installed on the bottom side of the pc assembly. JH1 and JH3 are mounted on the top side of the pc assembly. If mating 2mm female headers (4.3mm ht.) are used, the pc assembly will be about ¼″ above the mating pc board. This allows standard (0.250″) standoffs to be used with the corner mounting holes if desired. The hole size is 2.3mm – suitable for 2-56 or M2 screws.



- JH1 – JTAG (connects to external ICE)
- JH2 – DAI, DPI, I/O, SPI & System
- JH3 – Clock & Boot Configuration)
- JH4 – Power & Ext Clock
- JH5, JH7 – Data Bus
- JH6 – Link Ports

Power Supply

There are two power supply connections to the dspblok: DSP core (Vdd) and DSP I/O and Memory (Vd+3.3). The DSP core supply may range from 3.3V to 5V. This is the input to an on-board switching power supply that supplies 1.1V to the ADSP-21469. DO NOT use a higher voltage supply for the core supply input (JH4-Vdd).

A single 3.3V supply is all that is required to power the dspblok 21469, but in some cases, a 5V supply may be more convenient. The DSP I/O and Memory supply must be 3.3V.

For example, a product may already have a switching supply that converts directly to 3.3V. In this case, it may be desirable to supply both the DSP core and the dspblok Vd+3.3 (I/O) from this supply.

Alternatively, a product might have a 5V supply (perhaps from an external power supply module). A simple LDO fixed regulator could be used to create 3.3V from this supply. Most high-speed devices, including the ADSP-21469, draw most of their power from their core supplies. In this scenario, it makes no sense to power the dspblok core with 3.3V since the LDO would be dissipating the excess voltage as heat. If the I/O requirements are modest, the power dissipation in the LDO might not be significant

Power consumption is largely a function of the operating clock of the ADSP-21469 and the computation tasks that are being executed on the DSP. The highest consumption occurs when the DSP is performing continuous floating point operations at maximum core clock (450MHz). Accessing external I/O such as the DRAM or other peripherals consumes less power in the benchmarks that we have performed. The following table shows power consumption measurements for a typical dspblok 21469 operating in a variety of configurations.

Typical Power Consumption

Core Clock	Continuous floating point operations	Mixed floating point & DAI operations	Mixed floating point & DDR2 operations	Continuous floating point operations	Mixed floating point & DAI operations	Mixed floating point & DDR2 operations
Vdd = 3.3V & Vd+3.3						
	mA	mA	mA	mW	mW	mW
100MHz	120mA	119mA	119mA	396mW	393mW	393mW
200MHz	150mA	148mA	147mA	495mW	488mW	485mW
400MHz	214mA	209mA	208mA	706mW	690mW	686mW
450MHz	231mA	225mA	225mA	762mW	743mW	743mW
Vdd = 5.0V						
	mA	mA	mA	mW	mW	mW
	Vdd = 5V Core Supply Only					
100MHz	60mA	59mA	54mA	300mW	295mW	270mW
200MHz	77mA	76mA	76mA	385mW	380mW	380mW
400MHz	111mA	108mA	108mA	555mW	540mW	540mW
450MHz	118mA	115mA	115mA	590mW	575mW	575mW
	Vd+3.3 Supply Only					
100MHz	35mA	35mA	35mA	116mW	116mW	116mW
200MHz	39mA	39mA	39mA	129mW	129mW	129mW
400MHz	48mA	48mA	48mA	158mW	158mW	158mW
450MHz	50mA	51mA	51mA	165mW	168mW	168mW
	Composite Vdd & Vd+3.3					
100MHz				416mW	411mW	386mW
200MHz				514mW	509mW	509mW
400MHz				713mW	698mW	698mW
450MHz				755mW	743mW	743mW

Memory

The ADSP-21469 includes an on board DDR2 DRAM controller. Unlike earlier SHARC processors, the DRAM interface is largely independent of the external data bus. On the dspblok 21469, the only overlap is MS0#, which is not available because its address is assigned to DDR2_CS#.

The dspblok 21469 uses a 1Gb (64M x 16) DDR2 DRAM. DDR2 memory is much faster and typically much larger than older SDRAM. PC board layout is non trivial. The dedicated DDR2 interface of the ADSP-21469 has been carefully laid out with respect to trace length, signal integrity, and bus isolation so that the DDR2 operates reliably at maximum speed. The CD includes examples of DDR2 register configuration code.

A 16Mbit serial flash memory may be used to bootload the DSP. There is a pre-installed bootloader program that resides in the flash. This program accepts standard ADI loader files (SPI, slave, binary, 8 bit) and can be uploaded with a dspblok power supply module, a dspstak 21469 or any Danville board that includes a USB transceiver. You can also boot via the UART. If you want to manage the flash memory yourself, you can overwrite the internal bootloader via the JTAG port. In this case, the Danville dspFlash™ Blackfin & SHARC Programmer is available for fast production programming.

64kbits of EEProm memory is also available as byte addressable user memory. For example, you might store serial numbers, build versions or calibration values in this space.

There are other Flash/EEProm combinations available via special order. Contact Danville if you have special memory requirement needs.

DAI & DPI

The ADSP-21469 has 20 DAI lines and 14 DPI lines. Collectively these can be thought of as two sets of crossbar switches that connect to a wealth of peripherals. The dspblok 21469 maintains the flexibility of the DAI and DPI by bringing out all 20 DAI and 12 of 14 DPI lines to external connections.

The DAI is completely unencumbered and can be assigned to I/O in an arbitrary manner. The DPI is slightly restricted in that the primary SPI interface is assigned to DPI1 (MOSI), DPI2 (MISO), DPI3 (SCK), DPI5 (Flash SS) and DPI6 (EE SS). With the exception of DPI6, these connections are necessary to support SPI master booting. The dspblok 21469 may also be booted from an external host using SPI slave mode. In this case DPI4 is also used as the SPIDS# line.

Data Bus

The dspblok 21469 brings out the complete asynchronous data bus including all address lines with the exception of MS0# which would be in conflict with the DDR2 chip select.

Clocks

The dspblok 21469 supports both internal and external clocking options. You can add a standard HC49 style crystal to the board for internal clocking or you can supply an external clock. The configuration header (JH3)

allows any ADSP-21469 power-up clock configuration to be set.

Link Ports

The dspblok 21469 has two link ports available that can be used to interface to additional dspblok 21469 boards or may be used to connect to other external devices such as FPGAs.

Multiprocessor Configurations

The dspblok 21469 may be used as a coprocessor in a larger system. Perhaps the easiest way to communicate with an external host to configure the secondary SPI port as a slave. The primary SPI port remains configured as an SPI master so that it can manage local resources such as flash and EE memory as well as other I/O devices.

Certainly, the Link Ports are available for multiprocessor systems. They are ideal where fast interprocessor communications are required. Since clocks and data are always driven from the same source, clock skew is minimized.

You can also use SPORTs for interprocessor communication. This can be a good approach for Blackfin – SHARC combinations. It also works well for multichannel applications where you might use several dspbloks to provide front end signal processing and combine into a consolidated TDM data stream. The results could be routed to a central processor that manages the whole system and communicates to the outside world.

Reset

On power up, the dspblok 21469 is automatically held in reset until the 3.3V power supply is stable. RESET# is active low and open drain. This means that an external device(s) may also reset the dspblok by pulling the reset line low. External devices should not drive RESET# high since this can cause contention with the on-board reset circuit. The external reset circuit is connected in a wired-OR configuration using an active low – open drain configuration. A 74LVC125 or an open collector/drain transistor circuit are possibilities. You do not need an additional pull up resistor.

Signal Levels

The dspblok 21469 uses standard 3.3V logic levels. These levels have become the defacto operating standard for many years now. DO NOT use 5V logic when interfacing to the dspblok. The inputs are not 5V tolerant. Most external devices requiring 5V TTL levels can be safely driven by the dspblok. If you have questions concerning interfacing external devices, please contact Danville for suggestions.

Boot Options

All ADSP-21469 boot options are available via the configuration and programming header (JH3). These include Master SPI (flash memory), Slave SPI (external host) or Link Port. The boot mode pins are pulled passively to create a default boot mode of SPI Master.

Connections

	Pin	Description			Pin	Description			Pin	Description
JH1		**JTAG**		**JH2**		**DAI, DPI, IO**		**JH3**		**Configuration**
	1	EMUSEL			1	GND			1	GND
	2	EMU			2	DPI8/IO0/SS1#		Note 4	2	BOOTCFG0
Note 1	3	Key (No Pin)		Note 2	3	DPI4/IO1/SS2#			3	Vd+3.3
	4	GND			4	DPI13/IO2/SS3#		Note 4	4	BOOTCFG1
	5	Vd+3.3 Mon			5	DPI14/IO3/SS4#			5	Vd+3.3
	6	TMS			6	FLG0/IO4/SS5#		Note 4	6	BOOTCFG2
	7	GND			7	DPI7/SS0#			7	Vd+3.3
	8	TCK			8	DPI11/I2C_SDA		Note 5	8	CLKCFG0
	9	GND			9	DPI12/I2C_SCL			9	GND
	10	TRST#			10	DPI9/UART_TX		Note 5	10	CLKCFG1
	11	GND			11	DPI10/UART_RX				
	12	TDI			12	FLG1		**JH4**		**Power**
	13	GND		Note 3	13	Reserved				
	14	TDO			14	DPI1/MOSI			1	GND
	15	Vd+3.3			15	DPI3/SCK			2	Ext Clk
	16	Vd+3.3			16	DPI2/MISO		Note 6	3	Vd+1.1
					17	RESET#			4	DSP ClkOut
				Note 3	18	Reserved			5	Vd+3.3
					19	DAI1			6	Vd+3.3
					20	DAI2		Note 7	7	Vdd (3.3V or 5V)
					21	DAI3		Note 7	8	Vdd (3.3V or 5V)
					22	DAI4			9	GND
					23	DAI5			10	GND
					24	DAI6				
					25	DAI7				
					26	DAI8				
					27	DAI9				
					28	DAI10				
					29	DAI11				
					30	DAI12				
					31	DAI13				
					32	DAI14				
					33	DAI15				
					34	DAI16				
					35	DAI17				
					36	DAI18				
					37	DAI19				
					38	DAI20				
					39	GND				
					40	GND				

	Pin	Description			Pin	Description			Pin	Description
JH5		**Data Bus**		**JH7**		**Address Bus**		**JH6**		**Link Port**
Note 8	1	NC		Note 8	1	NC			1	L0DAT0
Note 8	2	NC		Note 8	2	NC			2	L0DAT1
Note 8	3	NC		Note 8	3	NC			3	L0DAT2
Note 8	4	NC			4	A23			4	L0DAT3
Note 8	5	NC			5	A22			5	L0DAT4
Note 8	6	NC			6	A21			6	L0DAT5
Note 8	7	NC			7	A20			7	L0DAT6
Note 8	8	NC			8	A19			8	L0DAT7
Note 8	9	D7			9	A18			9	LCLK0
	10	D6			10	A17			10	LACK0
	11	D5			11	A16			11	L1DAT0
	12	D4			12	A15			12	L1DAT1
	13	D3			13	A14			13	L1DAT2
	14	D2			14	A13			14	L1DAT3
	15	D1			15	A12			15	L1DAT4
	16	D0			16	A11			16	L1DAT5
	17	RD#			17	A10			17	L1DAT6
	18	WR#			18	A9			18	L1DAT7
	19	ACK			19	A8			19	LCLK1
Note 8	20	NC			20	A7			20	LACK1
					21	A6				
					22	A5				
					23	A4				
					24	A3				
					25	A2				
					26	A1				
					27	A0				
					28	MS1#				
					29	MS2#				
					30	MS3#				

Note 1: Mating Plug is plugged to prevent misalignment.
Note 2: DPI4 also functions as SPIDS# in SPI slave booting applications.
Note 3: Leave Unconnected.
Note 4: Boot Configuration is 001 by default (SPI Master Booting).
Note 5: Clock Configuration is 10 by default (16 x ClkIn), generally reconfigured in program code.
Note 6: Vd+1.1 is for power supply monitor only (DSP Core supply).
Note 7: Vdd is externally supplied: 3.3 to 5V (Vin for DSP Core Switching supply). Both connections must be the same voltage.
Note 8: Not Connected, may be used for extended features by other dspbloks.

Connector Recommendations & Notes

Connector Specification

All dspblok connectors are gold plated 2mm dual row headers. Male connectors are generally mounted on the bottom side of the dspblok pc assembly. The exceptions are JH3 & JH1, which are not intended to mate to a motherboard. Mating female connectors are included for your target pc board. The plastic base of each male connector is 2mm. The height of the female headers is 4.3mm. This means that the inserted combined height of the two connectors is 6.3mm or approximately ¼ inch. Standard standoffs may be used to secure the dspblok to the target pc board. Mounting holes are 2.3mm dia. to accommodate a 2-56 or M2 screws or standoffs.

JH1 – JTAG

This connector is mounted on the top side of the dspblok. A 2mm right angle header is used instead of the larger ADI JTAG header. The connections on the JTAG header correspond with the connections on an ADI JTAG header. In addition, Vd+3.3 is also available. This addition allows an active buffer circuit to be added for JTAG chaining applications. Danville has an ADI JTAG adapter available (P/N A.08153).

The dspblok 21469+ICE omits JH1 since the debugger is on-board. If you want to use an external emulator or the Danville dspFlash Blackfin & SHARC Programmer, you may remove the ADI Debugger and use the JTAG connection provided below the debugger.

JH2 – DAI, DPI, IO

This connector is mounted on the bottom side of the dspblok. The DAI lines are all uncommitted by the dspblok. With the exception of the SPI lines, the DPI can be freely assigned. The alternate names in the table are dspstak I/O conventions. If you are using a dspstak for development, it may be prudent to following these usage conventions.

JH3 – Configuration

This connector is mounted on the top side of the dspblok. It provides direct access to the ADSP-21469 clock mode and boot mode configuration pins. In most cases, you should leave all the connections open. Use shorting jumpers if you want to change the configuration. Note that each shorting jumper will cause the corresponding mode pin to deviate from the pin state of the default configuration. This means that some pins are pulled high and others low.

JH4 – Power & Clock

This connector is mounted on the bottom side of the dspblok. This is the main power feed to the dspblok, Vdd is the input to the core switching supply. Both Vdd pins should be connected to together and fed with either 5V or 3.3V. Likewise, Vd+3.3 should be connected together and fed with 3.3V. Vd+1.1 is current limited by a large resistor. Its purpose is for diagnostics.

JH5, JH7 – Data Bus

The data bus is split to two separate connectors, one for address and the other for data. The ADSP-21469 has an 8 bit data bus. Earlier dspbloks based on the ADSP-21369 supported a 32 bit data bus. This was needed primarily to support wide SDRAM interfacing. The original JH6 connection on the dspblok 21369zx board was used for the extended data bus. This is also why there are unused pins on JH5. If you are adapting a dspblok 21369zx design to support the dspblok 21469, you should verify that these changes will not impact your design. In most cases, this will not be an issue.

The address bus is also organized so that the MS# lines and the lower address lines are grouped together. This allows a smaller receptacle to be used when the whole address space is not required.

For example, the dspstak 21469 uses a 16 pin receptacle for JH7. This frees up board space and simplifies routing on the mating pcb.

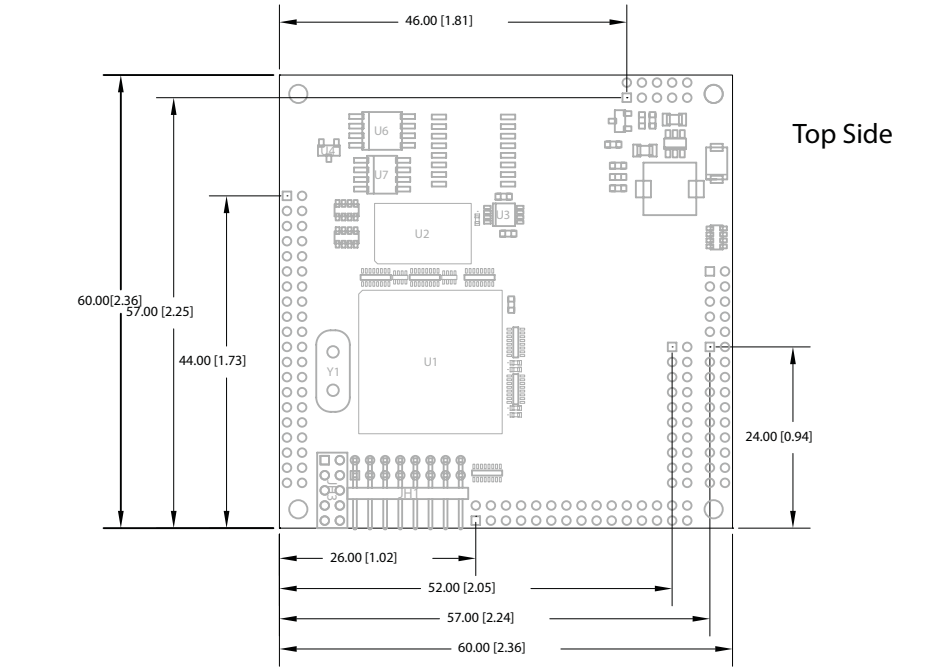
JH6 – Link Port

The Link Port connections include 33 ohm series terminators as well as 10K pulldowns for LCLKx and LACKx. The series terminators will have minimal effect when located on the receive side of a link port connection, but are required on the driving end of a link port connection.

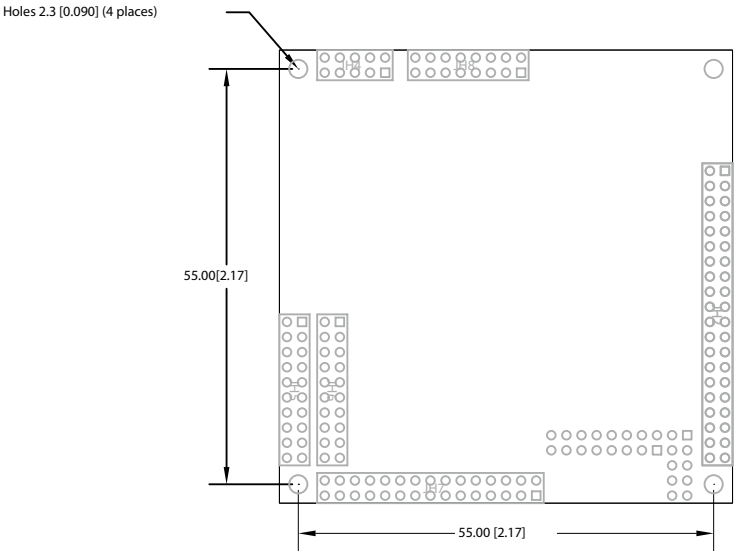
If you are connecting another non-dspblok device to a link port, make sure your circuit includes series terminators at the driving end of any connection. These terminators are often available internally in FPGAs. You should not supply additional terminators on the dspblok side of a connection.

Link ports circuits are fast so careful attention to pcb layout and/or cabling is essential. Consult a Danville engineer if you have questions about this topic.

Mechanical Dimensions (dspblok 21469)



Top Side

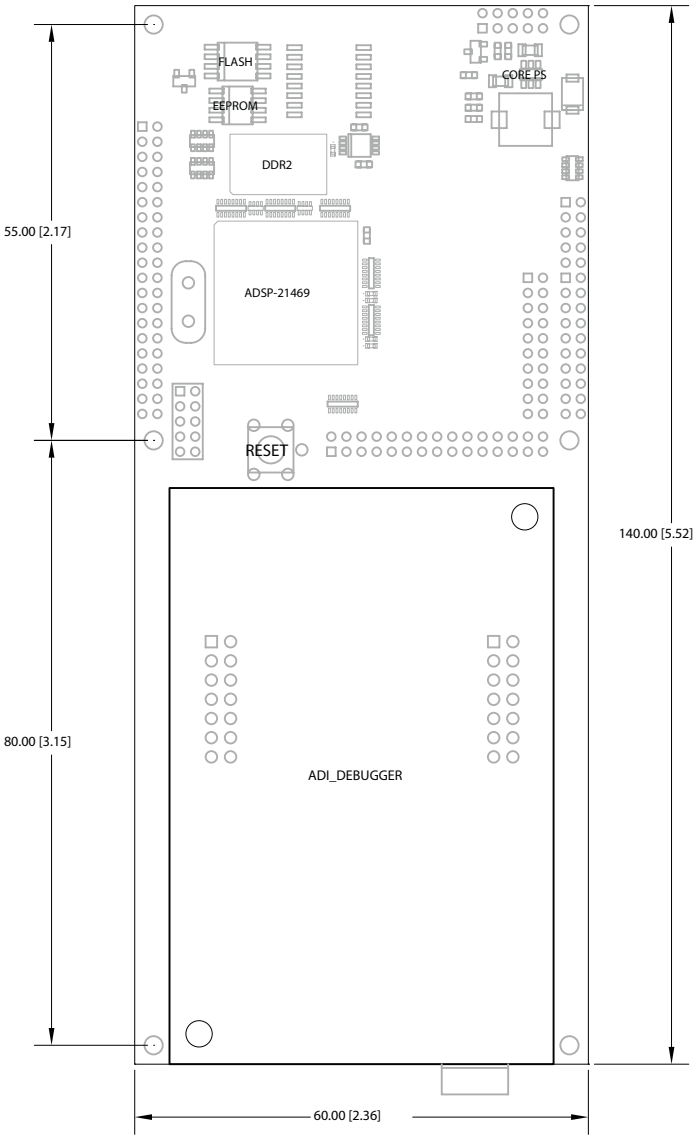


Bottom Side

Mounting holes are equidistant from the center of the dspblok. These holes are 2.3mm in diameter, suitable for 2-56 or M2 screws. When 4.3mm height mating female connectors are used, the board will be 6.3mm (0.25 in) above the target board, therefore 0.250 standoffs may be used.

Component height above the board is 6mm (0.236 in). The board is 1.6mm (0.062 in) thick.

Mechanical Dimensions (dspblok 21469+ICE)



The dspblok 21469+ICE board has identical mounting holes and mating connections as the production dspblok 21469. Two additional mounting holes are provided for support as shown.

The debugger portion of the dspblok 21469+ICE is power by a separate 5V 1A power supply. The connector is a 5.5/2.5mm center positive coaxial power jack located on the bottom of the drawing.

Manual Reset is also available via a tact switch located above the ADI debugger.

Schematic

The Distribution CD includes schematic diagrams of the dspblok 21469.

Product Warranty

Danville Signal Processing, Inc. products carry the following warranty:

Danville Signal Processing products are warranted against defects in materials and workmanship. If Danville Signal Processing receives notice of such defects during the warranty period, Danville Signal Processing shall, at its option, either repair or replace hardware products, which prove to be defective.

Danville Signal Processing software and firmware products, which are designated by Danville Signal Processing for use with our hardware products, are warranted not to fail to execute their programming instructions due to defects in materials and workmanship. If Danville Signal Processing receives notice of such defects during the warranty period, Danville Signal Processing shall, at its option, either repair or replace software media or firmware, which do not execute their programming instructions due to such defects. Danville Signal Processing does not warrant that operation of the software, firmware, or hardware shall be uninterrupted or error free.

The warranty period for each product is one year from date of installation.

Limitation of Warranty:

The forgoing warranty shall not apply to defects resulting from:

- Improper or inadequate maintenance by the Buyer;
- Buyer-supplied software or interfacing;
- Unauthorized modification or misuse;
- Operation outside the environmental specification of the product;
- Improper site preparation and maintenance.

Exclusive Remedies:

The remedies provided herein are the Buyer's sole and exclusive remedies. In no event shall Danville Signal Processing, Inc. be liable for direct, indirect, special, incidental or consequential damages (including loss of profits) whether based on contract, tort, or any other legal theory.

RoHS & WEEE Compliance

The European Union approved a directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment. This directive is commonly known as RoHS, EU Directive 2002/95/EC. This directive severely limits the amount of lead and 5 other substances that can be in contained in nonexempt products. The directive became European law in February 2003 and took effect July 1, 2006.

It is likely that other countries outside the European Union and some states in the United States may adopt similar legislation.

There are a number of important exemptions that affect many of our customers. The most important of these is Category 9, Control and Monitoring Instruments. You may wish to review your situation to see if this exemption applies to you. Military, medical and some other products are also exempt. We suggest that you make an appropriate assessment concerning your products.

The dspblok 21469 is RoHS compliant.

The dspblok 21469 is a subcomponent of a larger system; therefore it is not subject to the WEEE directive EU Directive 2002/96/EC.